Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 1 with the following amended paragraph:

~~For purposes of illustration, simplified drawings of two different diffussional fluid transport regimes associated with two different state of the art flow field designs (i.e., standard and interdigitated) have been provided as prior art FIGS. 1A and 1B, respectively.~~ For purposes of example, at higher current densities, the poor performance characteristics of conventional DMFC systems have been attributed to diffusion mass transfer limitations associated with fuel and oxidant delivery. ~~cite?~~

Please replace the paragraph beginning at page 5, line 7 with the following amended paragraph:

In addition to the foregoing, several different configurations and structures have been contemplated for direct liquid feed fuel cell systems such as, for example, a direct methanol electrode structure having a solid polymer electrolyte (SPE). Because such polymer electrolytes are typically cast as solid membranes, this type of electrode assembly is commonly referred to as a "membrane electrode assembly" (MEA). A typical MEA consists essentially of a proton conducting membrane (i.e., the solid polymer electrolyte) sandwiched between two platinum coated electrode structures. A significant problem, however, with DMFC systems having MEAs is a phenomenon known as "methanol cross-over." ~~As is depicted in prior art FIGURE 2,~~ methanol in conventional DMFC systems has a tendency to cross-over from the anode to the cathode via diffusion (i.e., it migrates through the electrolyte), where it adsorbs onto the cathode catalyst and reacts with oxygen from air resulting in a parasitic loss of methanol fuel and concomitant reduction in fuel cell voltage. Indeed, performance losses of 40-100 mV at a given current density have been observed at the cathode of DMFC systems utilizing a direct methanol feed (Potje-Kamloth et al., Abstract No. 105, Extended Abstracts 92-2, "Fall Meeting of the Electrochemical Society" (1992), Kuver et al., J Power Sources 52:77 (1994)).

Please delete the paragraph beginning at page 11, line 4, which starts with "Figure 1A."

Please delete the paragraph beginning at page 11, line 6, which starts with "Figure 1B."

Please delete the paragraph beginning at page 11, line 8, which starts with "Figure 2."

Please delete the paragraph beginning at page 11, line 10, which starts with "Figure 3."

Please delete the paragraph beginning at page 11, line 13, which starts with "Figure 4."

Please replace the paragraph beginning at page 11, line 16 with the following amended paragraph:

Figure ~~5~~ 1 illustrates a top exploded isometric view of a hydrodynamic transport structure integrally associated with an electrode assembly of a fuel cell system in accordance with an embodiment of the present invention.

Please replace the paragraph beginning at page 11, line 19 with the following amended paragraph:

Figure ~~6~~ 2 illustrates a top isometric view of the hydrodynamic transport structure integrally associated with the electrode assembly of Figure ~~5~~ 1.

Please replace the paragraph beginning at page 11, line 21 with the following amended paragraph:

Figure ~~7~~ 3 illustrates a side cross-sectional view taken along line ~~7-7~~ 3-3 of the hydrodynamic transport structure of Figure ~~6~~ 2.

Please replace the paragraph beginning at page 11, line 23 with the following amended paragraph:

Figure ~~8~~ 4 illustrates a side cross-sectional view taken along line ~~8-8~~ 4-4 of the hydrodynamic transport structure of Figure ~~6~~ 2.

Please replace the paragraph beginning at page 11, line 25 with the following amended paragraph:

Figure ~~9~~ 5 illustrates an exploded top isometric view of fluid transport and flow channel passageways associated with a fuel cell electrode stack assembly in accordance with an embodiment of the present invention.

Please delete page 12 in total.

Please delete the paragraph beginning at page 13, line 1 and ending at page 13, line 20.

Please replace the paragraph beginning at page 14, line 29 with the following amended paragraph:

Thus, and with reference to Figures ~~3-8~~ 1-5, the present invention is directed to a fluid delivery and removal channel passage structure integrally associated with an electrode structure 12 of a fuel cell system (not shown) such as, for example, (1) an anode of a bi-polar electrode plate assembly ~~(as best shown in Figure 3)~~ and (2) a cathode of a bi-polar electrode plate assembly ~~(as best shown in Figure 4)~~. ~~As shown in Figure 3,~~ The fluid delivery and removal channel passage structure comprises four fluid delivery channels 14 disposed across a first face 16 of the electrode structure 12. The fluid delivery channels 14 each preferably have dimensions of 10,000 μm (L) x 1,000 μm (W) x 100 μm (T). ~~As shown in Figure 4,~~ The fluid delivery and removal channel passage structure comprises an inlet port 28 and an outlet port 30 separated by a single porous bulk matrix fluid transport layer 32, wherein the porous bulk matrix fluid transport layer 32 is preferably defined by an array of interconnected linear acicular pores, and wherein the inlet and outlet ports 28, 30 are each adapted to transport fluid in a direction perpendicular to the longitudinal axes of the acicular pores. The porous bulk matrix fluid transport layer 32 preferably has dimensions of 10,000 μm (L) x 10,000 μm (W) x 100 μm (T).

Please replace the paragraph beginning at page 15, line 15 with the following amended paragraph:

As ~~best~~ illustrated ~~in Figure 7 and Figure 8,~~ the fluid delivery and removal channel passage structure also comprises at least one fluid removal channel 18 disposed across a second face 20 of the electrode structure 12 (wherein the second face parallely opposes the first face). The fluid removal channel 18 preferably has dimensions of 10,000 μm (L) x 10,000 μm (W) x 100 μm (T). The fluid removal channel 18 communicates with each of the fluid delivery channels 14 by way of four interposing porous bulk matrix fluid transport layers 22. The four interposing porous bulk matrix fluid transport layers 22 may be, for example, (1) an array of interconnecting linear acicular pores formed by selective anodic polarization of a silicon wafer in hydrofluoric acid (as described in further detail below), and/or (2) an interconnecting porous

matrix structure formed by the selective growth of a metal oxo polymer (as also described in further detail below).

Please replace the paragraph beginning at page 16, line 5 with the following amended paragraph:

In addition to the above-disclosed fluid delivery and removal channel structures (integrally associated with fuel cell electrode structures), the present invention is also directed to fuel cell electrode assemblies that comprise an anode structure in combination with a cathode structure, wherein such a configuration allows a flowing reactant/oxidant/electrolyte fluid to ionically connect the anode to the cathode. Accordingly, the present invention is further directed to a fluid transport passageway structure integrally associated and in combination with a bi-polar electrode plate assembly of a fuel cell system. The fluid transport passageway structure may be characterized in that the bi-polar electrode plate assembly comprises an anodic electrode structure bonded together with an opposing cathodic electrode structure ~~(best illustrated in Figures 5 and 6)~~.

Please replace the paragraph beginning at page 17, line 1 with the following amended paragraph:

The present invention is still further directed ~~(as best shown in Figure 9)~~ to fluid transport and flow channel passageway structures 70 associated with a fuel cell electrode stack assembly 72 (shown in exploded view). In this embodiment, the fuel cell electrode stack assembly comprises: (i) a first end cap assembly having a first fluid inlet port and second fluid outlet port; (ii) a second end cap assembly having a third fluid inlet port and a fourth fluid outlet port; and (iii) a plurality of bi-polar electrode plate assemblies interposed between the first and second end cap assemblies, wherein each of the bi-polar plate assemblies comprises an anodic electrode structure bonded together with an opposing cathodic electrode structure.

Please delete the paragraph beginning at page 20, line 20 and ending at page 20, line 23.

Please delete the paragraph beginning at page 29, line 10 and ending at page 29, line 12.

Please replace the paragraph beginning at page 30, line 8 with the following amended paragraph:

Thus, ~~and with reference to Figure 18,~~ the present invention is directed to a palladium blocking layer ~~10~~ integrally associated with an electrode structure ~~12~~ of a fuel cell system (not shown) such as, for example, a DMFC system. In this embodiment, the electrode structure ~~12~~ comprises an inorganic (i.e., noncarbonaceous) support substrate ~~14~~ having one or more discrete porous regions, wherein the one or more discrete porous regions is defined by an array of acicular pores ~~16~~ disposed across the top surface area of the electrode structure ~~12~~ such that at least a portion of the blocking layer ~~10~~ covers the top surface area and protrudes into the array of acicular pores ~~16~~ (note that the pores are preferably interconnected). As shown, the palladium blocking layer ~~10~~ is a substantially voidless metallic palladium membrane, and the support substrate ~~14~~ is porous silicon (e.g., a bulk silicon matrix having a plurality of acicular pores). Moreover, because of the crystalline nature associated with silicon and palladium, the support substrate ~~14~~ may be fusion bonded together with the palladium blocking layer ~~10~~ (optionally with an interposing metallic glue layer) such that the opposing crystalline lattices commingle.

Please replace the paragraph beginning at page 35, line 22 with the following amended paragraph:

This example discloses the processing steps associated with making a silicon-based electrode adapted for use with a fuel cell system in accordance with an embodiment of the present invention. In this example, the processing steps consist of (1) the anode fabrication steps, and (2) the cathode fabrication steps. Without limitation, the principal processing steps are set forth below ~~and with reference to FIGS. 23 to 52 and FIGS. 54 to 79~~.

Please replace the paragraph beginning at page 35, line 29 with the following amended paragraph:

ANODE FABRICATION – Start with a silicon substrate having the following characteristics: 400 μm double side polished, (100) crystal orientation, 0.005 to 0.10 Ω-cm, n-type, 100 mm diameter ~~(refer to Figure 23)~~, and process in accordance with the following steps:

Please replace the following paragraphs beginning at page 36, line 4 and ending at page 46, line 19 with the following amended paragraphs:

1.1 Deposit a 5000 Å +/-5% layer of silicon dioxide (dielectric) on the front and backside of the silicon substrate via wet thermal oxidation ~~(refer to Figure 24)~~.

1.2 Deposit 600 Å +/-5% of silicon nitride (dielectric) on the front and backside of the silicon substrate via LPCVD nitride deposition ~~(refer to FIG. 25)~~.

1.3 Deposit photoresist patterned from Mask A1-1F on the front side of the silicon substrate – the openings only expose the fuel and oxidant inlet/outlets, the dicing lanes, and the flow channels ~~(refer to FIGS. 26A and 26B)~~.

1.4 RIE both dielectrics on the front side of the silicon substrate ~~(refer to FIG. 27)~~.

1.5 Strip the photoresists from the front side of the silicon substrate ~~(refer to FIG. 28)~~.

1.6 Deposit photoresist patterned from Mask A1-2B on the backside of the silicon substrate – the openings only expose the fuel and oxidant inlet/outlets, the dicing lanes, and the flow channels ~~(refer to FIGS. 29A and 29B)~~.

1.7 RIE both dielectrics from the backside of the silicon substrate ~~(refer to FIG. 30)~~.

1.8 Strip photoresist from the backside of the silicon substrate ~~(refer to FIG. 31)~~.

1.9 KOH etch 150 μm from the front and backside of the silicon substrate-carve out the fuel and oxidant inlet/outlets, the dicing lanes, and the flow channels ~~(refer to FIG. 32)~~.

1.10 Sputter 200 Å of Ti – W followed by an additional 5000 Å of Au on the front side of the silicon substrate – for the anodic etching Ohmic contact ~~(refer to FIG. 33)~~.

1.11 Deposit photoresist patterned from Mask A1-3B on the backside of the silicon substrate – the openings only expose the fuel and oxidant inlet/outlets, the dicing lanes, and the "active" regions to anodic etching ~~(refer to FIGS. 34A and 34B)~~.

1.12 Anodic etch the silicon substrate – creating a 200 μm porous silicon layer ~~(refer to FIG. 35)~~.

1.13 Deposit photoresist patterned from Masks A1-4B on the backside of the silicon substrate – the openings only expose the fuel and oxidant inlet/outlets and the dicing lanes ~~(refer to FIGS. 36A and 36B)~~.

1.14 KOH etch out the porous silicon on the inlet/outlet plus electrical channels from the backside of the silicon substrate (quickly) – remove the porous silicon within the fuel and oxidant inlet/outlets and the dicing lanes ~~(refer to FIG. 37)~~.

1.15 Strip photoresist from the backside of the silicon substrate ~~(refer to FIG. 38)~~.

1.16 Remove the Ohmic contact for anodic etching from the front side of the silicon substrate ~~(refer to FIG. 39)~~.

1.17 Deposit photoresist patterned from Mask A1-1F (reused) on the front side of the silicon substrate – the openings only expose the fuel and oxidant inlet/outlets, the dicing lanes, and the flow channels ~~(refer to FIGS. 40A and 40B)~~.

1.18 RIE the remaining silicon material within the fuel and oxidant inlet/outlets and the dicing lanes from the front side of the silicon substrate ~~(refer to FIG. 41)~~.

1.19 Strip photoresist from the front side of the silicon wafer ~~(refer to FIG. 42)~~.

1.20 Selectively diffusion dope the porous silicon with phosphorous – to make the porous silicon conductive, approximately 50 mΩ-cm.

1.21 Deposit photoresist patterned from Mask A1-5F on the front side of the silicon substrate – the openings only expose the area for the electrical contacts between the porous silicon and the dicing lanes ~~(refer to FIGS. 43A and 43B)~~.

1.22 RIE both dielectrics from the front side of the silicon substrate ~~(refer to FIG. 44)~~.

1.23 Strip photoresists from the front side of the silicon substrate ~~(refer to FIG. 45)~~.

1.24 Sputter 200 Å Ti-W followed by an additional 4,800 Å Au on the front side of the silicon substrate – for the electrical contacts between the porous silicon and the dicing lanes ~~(refer to FIG. 46)~~.

1.25 Deposit photoresist patterned from Mask A1-6F on the front side of the silicon substrate – the photoresist covers the sputtered metal located on the front side of the substrate for negative metal lift off ~~(refer to FIGS. 47A and 47B)~~.

1.26 Etch Au and Etch Ti – W from the front side of the silicon substrate ~~(refer to FIG. 48)~~.

1.27 Strip the photoresists from the front side of the silicon substrate ~~(refer to FIG. 49)~~.

1.28 Remove the silicon nitride via RIE on both the front and backside of the silicon substrate ~~(refer to FIG. 50)~~.

1.29 Evaporate 600 Å of Ti – W followed by 2 μm of Au onto the backside of the silicon substrate ~~(refer to FIG. 51)~~.

1.30 Catalyst Deposition & Preparation:(a) Heat the silicon substrate to 200° C in air for 2 hours; (b) After the silicon substrate has cooled to RT, place silicon wafer in an aqueous ammonia solution of tetraamineplatinum(II) hydroxide hydrate, $[Pt(NH_3)_4](OH)_2$-xH_2O, at pH 8.5 and stir for 10 hours. The solution will contain enough platinum complex to deposit a maximum of 2% weight platinum on silicon, i.e., a 100 mg wafer will be placed in a bath containing 2 mg of platinum (3.4 mg tetraamineplatinum(II) hydroxide hydrate); (c) Remove the silicon wafer from the aqueous ammonia solution and dry *in vacuo* for 1 hour; (d) Heat silicon substrate under a flow of oxygen/nitrogen (20:80) from RT to 400°C at a rate of 2°C per minute, approximately 3 hours, and then hold at 400°C for 1 hour; (e) After the silicon wafer has cooled to RT, placed silicon wafer in an aqueous ammonia solution of hexamineruthenium(III) chloride, $[Ru(NH_3)_6]Cl_3$, at pH 8.5 and stir for 10 hours. The solution will contain enough ruthenium complex to deposit a maximum of 1.5% weight ruthenium on silicon, i.e., a 100 mg wafer will be placed in a bath containing 1.5 mg ruthenium (4.6 mg hexamineruthenium(III) chloride); (f) Remove the silicon wafer from the aqueous ammonia solution and dry *in vacuo* for 1 hour; (g) Heat silicon substrate under a flow of oxygen/nitrogen (20:80) from RT to 400°C at a rate of 2°C per minute, approximately 3 hours, and then hold at 400°C for 1 hour; (h) Heat the silicon wafer under flowing hydrogen. The temperature should be rapidly increased from RT to 400°C at a rate of 25°C per minute, approximately 15 minutes, and held at 400°C for 4 hours ~~(refer to FIG. 52)~~.

~~The completed anode structure manufactured in accordance with the above processing steps is illustrated in FIGS. 53A and 53B, respectively.~~

CATHODE FABRICATION – Start with a silicon substrate having the following characteristics: 400 μm double side polished, (100) crystal orientation, to 1.0 Ωcm, n-type, 100 mm diameter ~~(refer to FIG. 54)~~, and process in accordance with the following steps:

2.1 Deposit a 1000 Å +/-5% layer of Stoichiometric silicon nitride on the front and backside of the silicon substrate via LPCVD nitride deposition ~~(refer to FIG. 55)~~.

2.2 Deposit photoresist patterned from mask C1-1B on the backside of the silicon substrate – to initially open inlet and outlet ports ~~(refer to FIGS. 56A and 56B)~~.

2.3 REI silicon nitride on the silicon substrate backside ~~(refer to FIG. 57)~~.

2.4 Isotropic or DRIE of 60-micron depth cavities from the backside of the silicon substrate – for the fuel and oxidant inlet/outlets and dicing lanes ~~(refer to FIG. 58)~~.

2.5 Strip the photoresists off the backside of the silicon substrate ~~(refer to FIG. 59)~~.

2.6 Remove all nitride on the backside of the silicon substrate by RIE (this fabrication step can be disregarded depending on stacking requirements) ~~(refer to FIG. 60)~~.

2.7 Sputter or evaporate 1 μm of aluminum on the backside of the silicon substrate – the aluminum will serve as an Ohmic contact for anodic etching ~~(refer to FIG. 61)~~.

2.8 Deposit photoresist patterned from Mask C1-2F on the front side of the silicon substrate – to open regions on the substrate for porous silicon etching ~~(refer to FIGS. 62A and 62B)~~.

2.9 RIE silicon nitride on the silicon substrate front side ~~(refer to FIG. 63)~~.

2.10 Strip the photoresists from the front side of the silicon substrate ~~(refer to FIG. 64)~~.

2.11 Anodic etch the silicon substrate – creating 50 μm porous silicon layer ~~(refer to FIG. 65)~~.

2.12 Strip off aluminum contact from the backside of the silicon substrate ~~(refer to FIG. 66)~~.

2.13 Selectively dope the porous silicon with phosphorus – to make the porous silicon conductive, approximately 50 mΩ-cm.

2.14 Anneal substrate to in N_2 – to drive in dopant and relieve stress inside the silicon substrate.

2.15 Sputter or evaporate 1 to 3 μm of aluminum on the front side of the silicon substrate – the aluminum serves as a thermal conductive layer for DRIE ~~(refer to FIG. 67)~~.

2.16 Deposit photoresists patterned from mask C1-3B on the backside of the silicon substrate – to initially open inlet, outlet ports and porous silicon for DRE, AZ4620, 12 μm ~~(refer to FIGS. 68A and 68B)~~.

2.17 Deep Reactive Ion Etching on the backside of the silicon substrate – anisotropic etching i.e., Bosch Etch ~~(refer to FIG. 69)~~.

2.18 Strip the photoresists off the backside of the silicon substrate ~~(refer to FIG. 70)~~.

2.19 Strip off aluminum contact from the front side of the silicon substrate ~~(refer to FIG. 71)~~.

2.20 Remove silicon nitride from the front side of the silicon substrate via RIE ~~(refer to FIG. 72)~~.

2.21 Sputter a seed layer of palladium on the front side of the silicon substrate – to be used to electroplate palladium for MeOH blocker ~~(refer to FIG. 73)~~.

2.22 Deposit photoresists patterned from mask C1-4F on the front side of the silicon substrate – to selectively deposit the palladium-blocking layer ~~(refer to FIGS. 74A and 74B)~~.

2.23 Pulse plate palladium as a MeOH blocking layer ~~(refer to FIG. 75)~~.

2.24 Strip the photoresist off the front side of the silicon substrate ~~(refer to FIG. 76)~~.

2.25 Deposit photoresists patterned from mask C1-5F on the front side of the silicon substrate and deposit photoresists to cover backside of the silicon substrate – to remove excess seed layer ~~(refer to FIGS. 77A and 77B)~~.

2.26 Remove excess palladium seed layer by chemical etch technique ~~(refer to FIG. 78)~~.

2.27 Strip the photoresists off the front side and backside of the silicon substrate ~~(refer to FIG. 79)~~.

2.28 Catalyst deposition and preparation:(a) Heat the silicon substrate to 200°C in air for 2 hours; (b) After the silicon substrate has cooled to RT, place silicon wafer in an aqueous ammonia solution of tetraamineplatinum(II) hydroxide hydrate, $[Pt(NH_3)_4](OH)_2$-xH_2O, at pH 8.5 and stir for 10 hours. The solution will contain enough platinum complex to deposit a maximum of 2% weight platinum on silicon, i.e., a 100 mg wafer will be placed in a bath containing 2 mg of platinum (3.4 mg tetraamineplatinum(II) hydroxide hydrate); (c) Remove the silicon wafer from the aqueous ammonia solution and dry *in vacuo* for 1 hour; (d) Heat silicon substrate under a flow of oxygen/nitrogen (20:80) from RT to 400°C at a rate of 2°C per minute, approximately 3 hours, and then hold at 400°C for 1 hour; (e) Heat the silicon wafer under flowing 1% H_2 in N_2. The temperature should be rapidly increased from RT to 400°C at a rate of 25°C per minute, approximately 15 minutes, and held at 400°C for 4 hours.

~~The completed cathode structure manufactured in accordance with the above processing steps is illustrated in FIGS. 80A, 80B and 80C, respectively.~~

EXAMPLE 2

SOL-GEL DERIVED ELECTRODE STRUCTURES

This example discloses the processing steps associated with making a sol-gel-based electrode assembly adapted for use with a fuel cell system. In this example, the processing steps consist essentially of (1) the anode fabrication steps, and (2) the cathode fabrication steps. ~~Without limitation, the principal processing steps are set forth below and with reference to FIGS. 81 to 153.~~

ANODE FABRICATION – Start with a silicon substrate having the following characteristics: (100) crystal orientation, 1 to 10 Ω-cm, n-type, 100 mm diameter, 300 +/-2 μm double side polished prime (DSPP), TTV<1 μm, and process in accordance with the following steps:

1.1 Grow 5000 Å, both sides of wet thermal oxide (SiO_2) on both sides of wafer. Deposit 600 Å, stoichiometric LPCVD silicon (Si_3N_4) on both sides of wafer ~~(refer to FIG. 81)~~.

1.2 Spin on AZ 1512 photoresist ~~(refer to FIG. 82)~~.

1.3 Expose with Photomask A2-1 F-KOH1 for front side ~~(refer to FIG. 83)~~.

1.4 RIE dielectrics on front side ~~(refer to FIG. 84)~~.

1.5 Strip photoresist and clean wafer ~~(refer to FIG. 85)~~.

1.6 KOH etch 100 μm in stirred 28% KOH, at 75°C ~~(refer to FIG. 86)~~.

1.7 Grow 3000 Å wet thermal oxide, (SiO^2) on exposed Si regions ~~(refer to FIG. 87)~~.

1.8 Deposit 600 Å of silicon nitride, Si_3N_4 ~~(refer to FIG. 88)~~.

1.9 Spin on AZ4620 photoresist on front side ~~(refer to FIG. 89)~~.

1.10 Expose with photo mask A2-2F-KOH2 for front side, which opens the front side patterns for active region for sol-gel ~~(refer to FIG. 90)~~.

1.11 RIE dielectrics down to bare Si on front side using CHF_3 and O_2. Strip photoresist and clean wafer ~~(refer to FIG. 91)~~.

1.12 KOH etch 100 μm in stirred 28% KOH, at 75°C ~~(refer to FIG. 92)~~.

1.13 Use photo mask A2-3F-PSPAD on front side, with AZ4620, for conductive strip ~~(refer to FIG. 93)~~.

1.14 RIE dielectrics 500 μm in width using CHF_3 and O_2 on front side to make PS strip ~~(refer to FIG. 94)~~.

1.15 Use photo mask A2-4B-OHMIC on back side with photoresist AZ1518 to create openings for ohmic contact for anodic etching ~~(refer to FIG. 95)~~.

1.16 RIE dielectrics on back side to bare Si using CHF_3 and O_2. Then strip photoresist and clean wafer ~~(refer to FIG. 96)~~.

1.17 Evaporate 1 μm Al on backside for anodic etching ohmic contact ~~(refer to FIG. 97)~~.

1.18 Anodic etch 50 μm (PS etch for macropores) in active region where sol-gel will be cast ~~(refer to FIG. 98)~~.

1.19 Wet etch Al ~~(refer to FIG. 99)~~.

1.20 Cast sol-gel precursor solution ~~(refer to FIG. 100)~~.

1.21 Heat treat at 120°C for 24 hours, pyrolyze at 450°C for 4 hours under flowing H_2 ~~(refer to FIG. 101)~~.

1.22 Evaporate 1 μm Al on backside as an RIE mask ~~(refer to FIG. 102)~~.

1.23 Use photo mask A2-5B-RIE1 on back side with photoresist AZ4620, to create offset right feed port ~~(refer to FIG. 103)~~.

1.24 Wet etch Al at port area on back side ~~(refer to FIG. 104)~~.

1.25 RIE dielectrics using CHF_3 and O_2 on back side at port opening ~~(refer to FIG. 105)~~.

1.26 RIE 100 μm Si on backside at port opening using SF_6 ~~(refer to FIG. 106)~~.

1.27 Strip photoresist and clean wafer ~~(refer to FIG. 107)~~.

1.28 Use photo mask A2-6B-DRIE on back side, with photoresist AZ4620, for DRIE shield ~~(refer to FIG. 108)~~.

1.29 Wet etch Al at port area on back side ~~(refer to FIG. 109)~~.

1.30 RIE dielectrics using CHF_3 and O_2 at port area on back side ~~(refer to FIG. 110).~~

1.31 DRIE to the dielectric interface on the front side ~~(refer to FIG. 111)~~.

1.32 Strip photoresist and clean wafer ~~(refer to FIG. 112)~~.

1.33 Use photo mask A2-7B-RIE2 with AZ4620 on the back side to expose Si for etching ~~(refer to FIG. 113)~~.

1.3 Wet etch Al ~~(refer to FIG. 114)~~.

1.35 RIE Si using CHF_3 and O_2 until porous silicon is reached, which is approximately 50 μm ~~(refer to FIG. 115)~~.

1.36 Strip photoresist and clean wafer ~~(refer to FIG. 116)~~.

1.37 Wet etch all Al ~~(refer to FIG. 117)~~.

1.38 Use photo mask A2-8B-LIFTOFF1 on the back side with AZ4620, to provide conductive layer and bonding interface ~~(refer to FIG. 118)~~.

1.39 RIE all of back side nitride (Si_3N_4) using CHF_3 and O_2 ~~(refer to FIG. 119)~~.

1.40 Evaporate Ti adhesion layer for successive Au layer on the back side ~~(refer to FIG. 120)~~.

1.41 Evaporate 2 μm of Au on back side ~~(refer to FIG. 121)~~.

1.42 Ti-Au lift-off using acetone ~~(refer to FIG. 122)~~.

1.43 Use photo mask A2-9F-LIFTOFF2 on the front side with AZ4620, to provide conductive layer and bonding interface ~~(refer to FIG. 123)~~.

1.44 RE dielectrics on front side using CHF_3 and O_2 ~~(refer to FIG. 124)~~.

1.45 REE dielectrics on front side ~~(refer to FIG. 125)~~.

1.46 Evaporate Ti adhesion layer for successive Au layer on front side ~~(refer to FIG. 126)~~.

1.47 Evaporate 2 μm of Au on front side ~~(refer to FIG. 127)~~.

1.48 Front side Ti-A side Ti-Au lift-off using acetone ~~(refer to FIG. 128)~~.

CATHODE FABRICATION – Start with a silicon substrate having the following characteristics: 300 μm double side polished, (100) crystal orientation, 1 to 1.0 Ω-cm, n-type, 100 mm (4") diameter, and process in accordance with the following steps:

2.1 Nitride Deposition – 1000 Å, S1 (front side) and S2 (back side).

2.2 Photo Mask C2_IF_PS for front side, S1, using photoresist AZ1512 ~~(refer to FIG. 129)~~.

2.3 Photo Mask C2_2B_OHMIC for backside, S2, using photoresist AZ1512 ~~(refer to FIG. 130)~~.

2.4 RIE nitride both front and backside ~~(refer to FIG. 131)~~.

2.5 Strip photo resists and clean wafer ~~(refer to FIG. 132)~~.

2.6 Evaporate 1 μm of Al on backside, S2 ~~(refer to FIG. 133)~~.

2.7 Isotropic etch: HF: HNO_3:CH_3COOH, etch out 200 μm Si ~~(refer to FIG. 134)~~.

2.8 Anodic etch 50 μm porous structure on front side ~~(refer to FIG. 135)~~.

2.9 Cast sol-gel precursor solution ~~(refer to FIG. 136)~~.

2.10 Heat treat at 120°C for 24 hours ~~(refer to FIG. 137)~~.

2.11 Pyrolyze at 500°C for 4 hours under flowing H_2.

2.12 Spin on photoresist on front side, S1, using photoresist AZ4620 ~~(refer to FIG. 138)~~.

2.13 Photo mask C2_3B_OFFSET, S2, using photoresist AZ4620.

2.14 Etch Al ~~(refer to FIG. 139)~~.

2.15 RIE 100 μm with SF_6 ~~(refer to FIG. 140)~~.

2.16 Photo Mask C2_4B_DRIE, S2, using photoresist AZ4620 ~~(refer to FIG. 141)~~.

2.17 DRIE 200 μm ~~(refer to FIG. 142)~~.

2.18 Strip photoresist on both sides, S1 and S2 ~~(refer to FIG. 143)~~.

2.19 Strip Al ~~(refer to FIG. 144)~~.

2.20 RIE nitride front side, S1 ~~(refer to FIG. 145)~~.

2.21 Sputter Pd 2000 Å on the front side, S1 ~~(refer to FIG. 146)~~.

2.22 Photo Mask C2_5F_PLATING ~~(refer to FIG. 147)~~.

2.23 Pulse plate Pd thin film ~~(refer to FIG. 148)~~.

2.24 Strip Photoresist and clean wafer ~~(refer to FIG. 149)~~.

2.25 Photo Mask C2_6F_PDETCH ~~(refer to FIG. 150)~~.

2.26 Etch Pd ~~(refer to FIG. 151)~~.

2.27 RIE dielectrics on backside (if required for bonding) ~~(refer to FIG. 152)~~.

2.28 Sputter external electrical connections on backside (if required for bonding) and (a) sputter 500 angstrom TiW and (b) Sputter 2 μm Au for metal connects ~~(refer to FIG. 153)~~.